Possible physical realization of a self-teaching neuron network

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A physical realization of a self-taught relationship between neuron-like elements is proposed.

Hopfield's model[2] of a neuron network has recently been discussed widely in the physics literature (e.g., Ref. 1). In this model, the *n*th neuron is described by a variable V_n which takes on the values 0 and 1. The time evolution of V_n is described by the equation

$$V_n(t+\Delta t) = \Theta(\sum_m J_{nm} V_m(t) - U_0), \tag{1}$$

where $\Theta(x)$ is the unit step function, J_{nm} is the relationship between the neurons, and U_0 is the neuron excitation threshold. In addition to the rapid evolution of V_n described by (1), there is a slow change in the relationships J_{nm}:

$$\Delta J_{nm} = C(2V_n - 1)(2V_m - 1)\Delta t, \quad C > 0. \tag{2}$$

Substantial changes in J_{nm} occur only if the configuration V_n is held constant for a long time (the teaching process). The evolution described by (1) takes the system from a arbitrary initial state and puts it in one of the configurations which was stored as a result of the teaching (this is pattern recognition).

Hopfield's model might serve as the operating principle of a new generation of computers. Such neurocomputers are in fact already in use,[3] but the teaching which goes on in them is carried out by means of a special synaptic-memory unit which is based on the principles of an ordinary computer. The development of a pure neurocomputer would require the physical realization of a teachable relationship between neurons [see Eq. (2)]. In the present letter we wish to propose one way to solve this problem.

We assume that the *n*th neuron (Fig. 1) is a logic element with *N* inputs (dendrites) and one output (an axon).[4] A voltage V_{mn} from the *m*th neuron arrives at the *m*th input. The voltage at the output is

$$V_n = \Theta(\sum_m V_{mn} - U_0). \tag{3}$$

(This characteristic could be arranged by means of a series connection of a voltage summer and a flip-flop.) Voltages W_{nm} and a reference voltage W_n are taken from voltage dividers (terminal filaments) at the output of the neuron. The voltage differ-

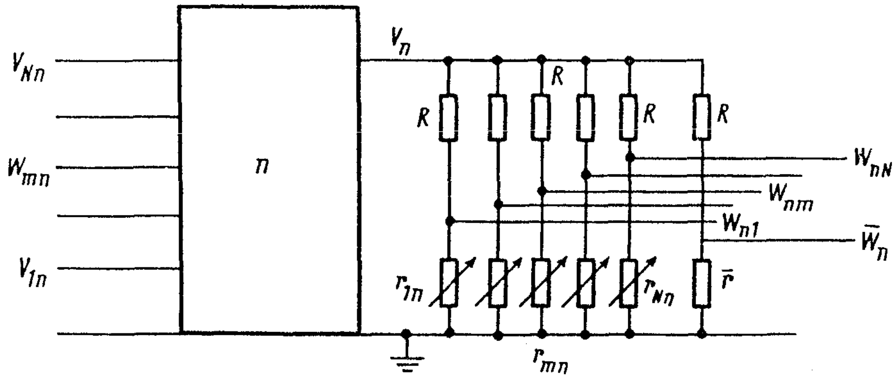

FIG. 1.

ence $V_{nm} = W_{nm} - \overline{W}_n$ is fed to the nth input of the mth neuron. Assuming $R \gg r_{nm}$, $\bar{r}$, we find $V_{nm} = \Delta r_{nm} V_n / R$, where $\Delta r_{mn} = r_{nm} - \bar{r}$ and, by virtue of (3), $V_n = \Theta(\Sigma_m \Delta r_{nm} V_m / R - U_0)$. To establish the analogy with Hopfield's model [see (1)], we should set

$$\Delta r_{nm}/R = J_{nm}. \tag{4}$$

If a teaching is to be realized [see Eq. (2)], the resistances r_{nm} must vary linearly in time with a coefficient which depends on V_m and V_n. This situation can be arranged by means of the circuit in Fig. 2. As r_{nm} we use the channel resistance of a field-effect transistor, which we have drawn here as a metal-insulator-semiconductor (MIS) structure for clarity and also to stress the point that the circuit of capacitor C is totally disconnected from the neuron inputs and outputs. The resitance r_{nm} depends on the voltage U_{nm} across capacitor C:

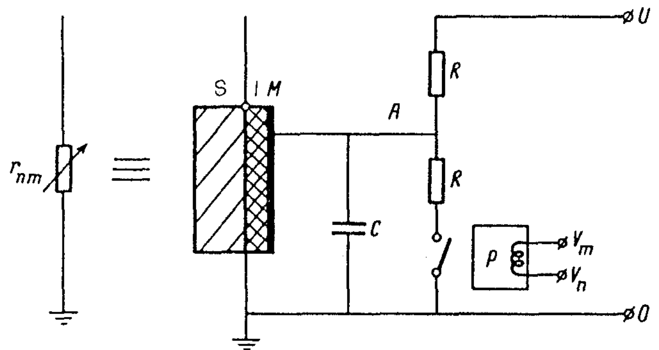

FIG. 2.

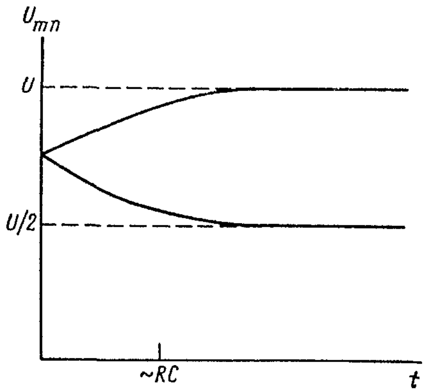

FIG. 3.

$$r_{nm} = f(U_{nm}), \tag{5}$$

where $f(U)$ is a function which decreases monotonically (with increasing U_{nm}, the density of the 2D electron gas in the MIS structure increases, and r_{nm} decreases). Capacitor C is the element which stores the information (in the form of a charge) on J_{nm} obtained in the course of the teaching.

The voltages V_n and V_m from the outputs of the nth and mth neurons are fed to a relay[1)] (Fig. 2). When the relay is off, the equilibrium voltage across capacitor C is U; when the relay is on, this voltage is $U/2$. We put the working point of the capacitor at the midpoint, i.e., at $U_{nm} = 3U/4$; then U_{nm} will vary in time, tending toward U or $U/2$ (Fig. 3). We assume that the time constant $\tau = \mathrm{RC}$ is long enough that the change in U_{nm} is slow. For $\Delta t \ll \tau$ we then have $U_{nm} = 3U/4 \pm \Delta t U/\tau$, where the upper and lower signs correspond to the cases with the relay off and on. Setting $\bar{r} = f(3U/4)$ and linearizing (5), we find

$$\Delta r_{nm} = \mp A \Delta t \quad (A > 0). \tag{6}$$

Let us assume that relay P is normally on. In the cases $V_n = 1$, $V_m = 1$ and $V_n = 0$, $V_m = 0$, no current is flowing through the relay, and we should take the lower sign in (6). In the cases $V_n = 0$, $V_m = 1$ and $V_n = 1$, $V_m = 0$ the relay is disconnected by the current flowing through it, and we need to take the upper sign in (6). We thus have

$$\Delta r_{nm} = A(2V_n - 1)(2V_m - 1)\Delta t\,. \tag{7}$$

By virtue of (4), the change in J_{nm} is the same as in Hopfield's model [see (2)]. Consequently, as long as the excursion from the working point is only small, the system proposed here is completely equivalent to Hopfield's model. For long teaching times, the linear dependence on t in (2) gives way to a saturation. However, the same is true of a real neuron network, and this effect has some useful consequences.[2]

It was suggested above that the recognition and teaching occur simultaneously (as in a real biological system), the only difference being a difference between the rates of the processes. However, one might envision some special regimes for recognition and teaching. In the recognition regime, capacitor C would be disconnected from the voltage divider at point A. The information storage time would then be determined only by charge leakage from capacitor C. Theoretically, this time could be made arbitrarily long, through the use of wide-gap insulators and low temperatures. The storage times attainable at the present state of the art (for reasonable dimensions of capacitor C) are sufficient for use in a working memory.

For long-term storage of the information, the unit with the field-effect transistor and the capacitor could be replaced by a memory cell.[5] The latter would be an MIS structure whose insulating layer would be fabricated in a special way and which would contain many localized states in its band gap. When a high voltage is applied to the gate, the charge carriers penetrate into the insulator and occupy localized states. After the external voltage has been removed, the trapped charge determines the voltage U_{nm}, on the gate of the MIS structure. This voltage controls the resistance (r_{nm}) of the channel of this structure. The time over which information could be stored in this case would be essentially unlimited, but the number of "reteaching" events would be limited (to $\sim 10^6$).

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[1)]There are various contactless methods to realize the relay: by using AND and OR logic circuits, by using a diode bridge and a field-effect transistor, etc.

[1]*Collection of Papers of Scientific and Technological Progress. Series on Physics and Mathematical Models of Neuron Networks*, Vol. 1, VINITI, Moscow, 1990.
[2]J. J. Hopfield, Proc. Nat. Acad. Sci. USA **79**, 2554 (1982).
[3]F. V. Shirokov, in *Collection of Papers of Scientific and Technological Progress. Series on Physics and Mathematical Models of Neuron Networks*, VINITI, Moscow, 1990, p. 229.
[4]W. S. McCullock and W. Pitts, in *Automata Studies* (ed. C. E. Shannon and J. McCarthy), Princeton Univ. Press, Princeton, NJ, 1956.
[5]*Proceedings of the Lebedev Physics Institute*, Vol. 184, Nauka, Moscow.

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